AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A processing system comprising a plurality of processing elements, the processing elements comprising a controller and computation means, the plurality of processing elements being dynamically reconfigurable by a cluster control signal as mutually independently operating task units that ~~which task units~~ comprise one processing element or a cluster of two or more processing elements~~-~~, the processing elements within a cluster being arranged to execute instructions under a common thread of program control, wherein the cluster control signal is derived from intermediate control signals transmitted through a reconfigurable channel infrastructure connected to the processing elements, wherein the reconfigurable channel infrastructure comprises a control chain with combination elements for each processing element and a switch between each pair of neighboring processing elements for locally controllably inhibiting transmission of intermediate control signals to a preceding or a succeeding processing element.

2. (Original) Processing system according to claim 1, wherein processing elements organized in a task unit share at least one common control signal for controlling instruction execution.

3. (Original) Processing system according to claim 2, wherein the common control signal is a flag controlling a guarded operation.

4. (Original) Processing system according to claim 3, wherein the guarded operation is a conditional jump.

5. (Currently amended) Processing system according to claim 1, wherein the processing elements are connected to each other via data-path connections ~~(DPC)~~.

6. (Currently amended) Processing system according to claim 5, wherein the data-path connections ~~(DPC)~~ are limited to neighbor-to-neighbor connections.

7. (Canceled).

8. (Currently Amended) Processing system according to claim 7, wherein the common control signal is derived by combining the intermediate control signals through a combination element~~,~~ associated ~~to~~ with each processing element.

9. (Currently Amended) Processing system according to claim 8, wherein the combination ~~elements consist~~element consists of an ~~OR-gates~~OR-gate.

10. (Currently Amended) Processing system according to claim 7, wherein the reconfigurable channel infrastructure comprises programmable sum-terms.

11. (Currently Amended) Processing system according to claim 7, wherein the reconfigurable channel infrastructure comprises programmable product-terms.

12. (Currently Amended) Processing system according to claim 7, wherein the reconfigurable channel infrastructure comprises mutually transverse chains.

13. (Currently Amended) Processing system according to claim 12, wherein the combination elements are arranged in chains having a first orientation and chains having a second orientation, and wherein the intermediate control signals transmitted through the chains having the ~~a~~ first orientation are forwarded to the combination elements in the chains having the ~~a~~ second orientation.

14. (Original) Processing system according to claims 13, wherein the intermediate control signals transmitted through the chains having the second orientation are forwarded to the combination elements in the chains having the first orientation.

15. (Canceled).

16. (Original) Processing system according to claim 15, wherein the combination elements consist of OR-gates.

17. (Original) Processing system according to claim 15, wherein the programmable switches comprise AND-gates.

18. (Previously Presented) Processing system according to claims 15, wherein the programmable switches are programmed by signals stored in memory cells.

19. (Original) Processing system according to claim 18, wherein at least one of the processing elements can write to at least one of the memory cells.

20. (Original) Processing system according to claim 18, wherein a set of memory cells used to program the switches is organized as a data-word in a memory.

21. (Original) Processing system according to claim 20, wherein the memory contains multiple data-words, and wherein the programmable switches are programmed by selecting one of these data-words.

22. (Original) Processing system according to claims 21, wherein one or more of the processing elements can program the programmable switches by dynamically selecting the data-word in memory.

23. (Currently Amended) Processing system according to claims 18, wherein the memory consists ~~consisting~~ of volatile random access memory ~~(RAM)~~.

24. (Currently Amended) Processing system according to claim 1, wherein ~~the processing elements comprise VLIW processors~~each single processing element is capable of executing a VLIW instruction.

25. (Currently Amended) Processing system according to claim 24, wherein the VLIW processors comprise an internal interconnect network ~~(IN)~~.

26. (Currently Amended) Processing system according to claim 25, wherein the internal interconnect network ~~(IN)~~ consists of point-to-point connections.

27. (Currently Amended) Processing system according to claim 25, wherein the internal interconnect network ~~(IN)~~ comprises data-path connections ~~(DPC)~~ going across operation issue slots within the processing elements.

28. (Original) Processing system according to claim 1, wherein the processing elements are arranged in a 2-dimensional grid.

29. (Currently Amended) Method for operating a processing system comprising a plurality of processing elements, the processing elements comprising a controller and computation means, the method comprising the steps of:

combining an intermediate control signal with an operation control signal of a processing element and selectively passing the combined signal to a further processing element,

deriving a cluster control signal from an operation control signal and two or more intermediate control signals, and

dynamically reconfiguring a processing element by the cluster control signal thereby dynamically reconfiguring~~according to whichmethod~~ the plurality of processing elements ~~are dynamically reconfigured~~ as mutually independently operating task units~~, which task units~~ that comprise one processing element or a cluster of two or more processing elements, wherein the processing elements within a cluster execute instructions under a common thread of program control.